In the Specification:

1. Please replace the paragraph at page 7, line 28 through page 8, line 2 with the following paragraph:

Fig. 5 is a ~~cross-sectional~~ top view of a semiconductor device test pattern according to firsts embodiment of the present invention. The semiconductor device test pattern may be formed on a semiconductor substrate such as a silicon substrate **100**. As shown in **Fig. 5**, a plurality of elongated word lines **140** (providing common gate structures for pluralities of memory cell transistors) are arranged parallel to each other on the semiconductor substrate **100**. In the embodiment depicted in **Fig. 5**, the word lines **140** are arranged in the vertical direction, although it will be appreciated that other orientations may also be used.

2. Please replace the paragraph at page 18, lines 20-25 with the following paragraph:

A first bit line **225** is electrically connected to a first probing pad **425** and is arranged at a right angle to the elongated axis of the active regions **135**. A second bit line ~~225~~ **255** is electrically connected to a second probing pad **525** and is parallel to the first bit line **225**. The second bit line **255**, as described later, may be electrically connected to each of a plurality of second self-aligned contact pads **185b** in the cell array region A.

3. Please replace the paragraph at page 18, lines 26-28 with the following paragraph:

The first impurity doped regions **155a** are electrically connected to the first bit line **225** in the cell array region A, and the second impurity doped regions ~~225~~ **155b** are electrically connected to the second bit line **255** in the cell array region A.

4. Please replace the paragraph at page 19, lines 5-19 with the following paragraph:

The second bit line **255** is electrically connected through the second self-aligned contact pads **185b** and the second direct contacts **245** to the second impurity regions **155b**. Specifically, the second self-aligned contact pads **185b** are electrically connected to respective of the second impurity regions **155b** and formed in a discontinuous state between the word

lines **145**. As shown in **Fig. 23**, the second self-aligned contact pads **185b** are electrically connected to one of the second impurity doped regions **155b** in a first active region **135**, as well as to one of the second impurity doped regions **155b** in a neighboring active region **135**. The self-aligned contact pads **185b** may be formed of a conductive material such as impurity doped polysilicon so that they operate as conductors. The second self-aligned contact pads **185b** may be electrically connected to the second bit line ~~**225**~~ **255** through the second direct contacts **245**. The second direct contacts **245** may be a kind of contact plug that are electrically connected to storage nodes. The second bit line **255** may be electrically connected through a second metal contact **505** to the second probing pad **525** in an outer region B_2.